UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,775	07/17/2003	Edison Fong	VEON-500 [FOV-123]	1682

7590 02/07/2005

Alfred A. Equitz
GIRARD & EQUITZ LLP
Suite 1110
400 Montgomery Street
San Francisco, CA 94104

EXAMINER	
DEB, ANJAN K	

ART UNIT	PAPER NUMBER
2858	

DATE MAILED: 02/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/621,775	FONG ET AL.	
	Examiner	Art Unit	
	Anjan K Deb	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 54-61* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 54-61* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1,54 are rejected under 35 U.S.C. 102(b) as being anticipated by Kozlowski et al. (US 6,417,504 B1).

Re claims 1, 54 Kozlowski et al. disclose (Fig. 1-3) sensing apparatus and method, including at least one sensor cell (PD1) configured to produce a sensor current (photoelectric charge) indicative of a sensed value and a readout circuit having an input node coupled to receive the sensor current, wherein the readout circuit also includes an output node (OUT) and output voltage generation circuitry (A2) between the input node and the output node (OUT), wherein the output voltage generation circuitry (A2) is configured to generate an output voltage (OUT) indicative of the sensed value in response to the sensor current (PD1) while clamping (voltage across Cclamp effectively clamped) the input node at a potential that is at least substantially fixed (column 4 lines 15-30).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-5, 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kozlowski et al. (US 5,929,434).

Re claims 1, 54 Kozlowski et al. discloses (Fig. 1-3) sensing apparatus and method, including at least one sensor cell (photodetector 10) configured to produce a sensor current I_{det} indicative of a sensed value and a readout circuit (14) having an input node 27 coupled to receive the sensor current, wherein the readout circuit also includes an output node (OUT) and output voltage generation circuitry (16,26,14) between the input node 27 and the output node (OUT), wherein the output voltage generation circuitry (16,26,14) is configured to generate an output voltage (OUT) indicative of the sensed value in response to the sensor current (I_{det}).

Kozlowski did not expressly discloses clamping the input node at a potential that is at least substantially fixed, but would have been obvious to do so since Kozlowski disclosed that the amplifier 16 connected between input 27 stabilizes the voltage at node 27 for a given flux so that it is insensitive to the noise of load FET.

At the time of the invention it would have been obvious for one of ordinary skill in the art to modify Kozlowski by adding clamping the input node at a potential that is at least

substantially fixed so that it is insensitive to the noise of load FET thereby enabling photon readout sensitivity (see abstract).

Re claims 2,3, Kozlowski discloses sensing apparatus includes at least one circuit element is a load transistor (70) coupled to the differential pair (differential amplifier)(Fig. 6)

Re claim 4, Kozlowski discloses voltage generation circuitry includes op-amp (16) configured to provide feedback from output of the op-amp to the input node.

Re claims 7, 55-56, 58 Kozlowski disclosed all of the claimed limitations as set forth above including input node coupled by a column line to sensor cell, and output voltage generation circuitry includes a readout capacitor (Vc) coupled to the output node (OUT), and the output voltage generation circuitry is configured to charge a readout capacitor 50 to a voltage indicative of the sensed value while clamping the input node 38 at a potential that is at least substantially fixed.

Re claims 59-61, Kozlowski disclosed all of the claimed limitations as set forth above including generating mirror current (I_{sig}) greater than sense current (I_{det}) (Fig. 2,4).

5. Claims 5,6, are rejected under 35 U.S.C. 103(a) as being unpatentable over Kozlowski et al. (US 5,929,434) in view of Champlin (US 4,816,768).

Re claims 5,6 Kozlowski disclosed all of the claimed limitations as set forth above except op-amp has inverting and non-inverting input.

Champlin discloses op-amp (amplifier A1) has inverting and non-inverting input, and at least one circuit element is a transistor Q1 having a channel terminal coupled to the inverting input (through resistor R4, R5) and a gate coupled to the output of the op amp (amplifier A1)(column 5 lines 55-67)(Fig. 2).

At the time of the invention it would have been obvious for one of ordinary skill in the art to modify Kozlowski by adding transistor gate connected to amplifier output and by connecting a transistor channel to the input of amplifier disclosed by Champlin so that the inverting (-) and non-inverting (+) input of amplifier assume the same dc bias voltage (Champlin: column 5 lines 55-67).

6 . Claims 7, 55-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kozlowski et al. (US 5,929,434) in view of Shinohara (US 6,791,613 B2).

Re claims 7, 55-58 Kozlowski et al. disclosed all of the claimed limitations as set forth above except input node coupled by a column line, and output voltage generation circuitry includes a readout capacitor coupled to the output node, and the output voltage generation circuitry is configured to charge a readout capacitor to a voltage indicative of the sensed value while clamping the input node at a potential that is at least substantially fixed.

Shinohara discloses (Fig. 8) input node sensor coupled by a column line (49,50) and output voltage generation circuitry includes a readout capacitor coupled to the output node, and the output voltage generation circuitry is configured to charge a readout capacitor 63 to a

voltage 52 indicative of the sensed value while clamping (clamping potential) the input node at a potential that is at least substantially fixed.

At the time of the invention it would have been obvious for one of ordinary skill in the art to modify Kozlowski et al. by adding input node coupled by a column line and output voltage generation circuitry including a readout capacitor coupled to the output node, and the output voltage generation circuitry configured to charge a readout capacitor disclosed by Shinohara for charging the capacitor to a voltage indicative of the sensed value.

Response to Arguments

7. Applicant's arguments with respect to claims 1-7, 54-61 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

White (US 3,781,574) discloses readout circuit for sensing current from a CCD array device.

Gowda (US 5,898,168) disclose image sensor comprising readout circuit for measuring photodiode current (Fig. 7).

Woolaway (US 6,344,651 B1) sensing current by differential current amplifier comprising transimpedance amplifiers to maintain a constant input potential (clamping input potential).

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Anjan K. Deb whose telephone number is 571-272-2228. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, N. Le, can be reached at (571) 272-2233.

Anjan K. Deb
Patent Examiner
Art Unit: 2858
2/3/05

Tel: 571-272-2228
Fax: 571-273-2228
E-mail : anjan.deb@uspto.gov